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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PHAM, THOMAS K	
ART UNIT	**PAPER NUMBER**
2121	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/944,776	KOCEV ET AL.	
	Examiner	Art Unit	
	Thomas K Pham	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. This action is in response to request for re-consideration filed on 12/30/2004.

2. Applicant's arguments with respect to claims 13-41 have been considered but they are not persuasive.

Quotations of U.S. Code Title 35

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim Rejections - 35 USC § 103

7. Claims 13-16, 18, 20-21 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,864,679 ("Kanai") in view of U.S. Patent No. 6,718,413 ("Wilson") and further in view of U.S. Patent no. 6,219,734 ("Wallach").

Regarding claims 13, 15 and 21

Kanai teaches a system for programmably allocating system resources to accommodate I/O transactions at I/O ports of a multiprocessor computer system comprising: setting parameters [criteria] for routing transactions to the port (col. 5 lines 41-43, "routing each transaction ... extracted by the extracting means"). Kanai does not teach determining the number of devices being serviced via the ports; with respect to the numbers of devices at the ports, assigning resources to the ports; identifying at least one assemblies for hot swapping; and copying the contents of cache memories associated with the at least one identified assemblies. However, Wilson teaches determining the number of devices being serviced for the bus [via the ports] (col. 10 lines 34-38, "at each arbitration phase ... to re-select the host adapter"); and with respect to the numbers of devices at the ports, assigning devices [resources] to the ports (col. 6 lines 10-19, "The host adapter circuit 316 ... meet the SCSI specifications") for the purpose prioritizing the devices to reduce the number of interrupts. Furthermore, Wallach teaches identifying at least one assemblies for hot swapping (col. 17 lines 33-35, "the configuration manager 1100 ... that has been hotly added"); copy the contents of old adapter to the new added adapter [port and adapter since they are both providing communication to I/O devices] (col. 12 lines 61-63, "the configuration manager 500 reprograms ... same configuration as the old adapter") for the purpose of keeping track and allocates resources for every managed adapter. Therefore, it would

have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the system of Wilson with the system of Kanai because it would provide for the purpose prioritizing the devices to reduce the number of interrupts. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the system of Wallach with the system of Kanai because it would provide for the purpose of keeping track and allocates resources for every managed adapter [port].

Regarding claims 14 and 16

Wallach teaches assigning resources to the ports comprises at least one of assigning control registers to the ports, assigning direct memory access engines to the ports, assigning cache memory to the ports and assigning priorities among the transactions at the ports (col. 10 lines 58-61, "The configuration manager 500 ... adapter's configuration space registers").

Regarding claims 17 and 19

Kanai teaches a system determining the number and types of transactions anticipated at the ports, wherein the assignment of resources is further with respect to the numbers and types of transactions at the ports (col. 23 lines 14-28, "A position of the ... transaction has been received").

Regarding claims 18 and 20

Wallach teaches the at least one identified assembly has a memory system, and the method further comprises copying the states and status of the memory systems associated with at least one identified assembly (col. 9 lines 22-25, "The registers of an adapter 310 ... the status of the adapter").

Regarding claim 31

Wallach teaches the I/O bridge comprises at least one control register, the at least one control register having a plurality of fields, and at least one field of the control register being associated with a corresponding resource, and the method further comprises writing to a selected field of the at least one control register so as to modify the assignment of resources (col. 10 lines 57-61, "Once an adapter 310 ... configuration space registers").

8. Claims 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanai in view of Wilson and further in view of Wallach and further in view of U.S. Patent no. 6,243,778 ("Fung").

Regarding claim 22

Kanai, Wilson and Wallach teaches a system for allocating resources but do not teach assigning a plurality of direct memory access (DMA) engines for use in processing I/O transactions. However, Fung teaches a plurality of DMA resources for use to process a large amount of data (col. 15 lines 26-31, "Every DMA channel of the ... the most efficient way possible"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the DMA resources of Fung with the system of Kanai, Wilson and Wallach because it would provide for processing data faster in the most efficient way possible.

Regarding claim 23

Fung teaches apportioning a selected number of DMA engines to process a given transaction at a particular I/O port (col. 15 lines 37-40, "Transaction Interface 210 ... used by their own queue").

Regarding claim 24

Fung teaches apportioning at least one DMA engine to process at least one transaction at a port (col. 15 lines 32-40, "The standard procedure for the ... used by their own queue").

Regarding claim 25

Wallach teaches a system for allocating resources identified as servicing multiple I/O devices (col. 4 line 64 to col. 5 line 5, "hot adding a programmable ... the I/O devices and the operational computer") and Fung teaches apportioning one DMA engine to process a given transaction at a port (col. 15 lines 32-40, "The standard procedure for the ... used by their own queue").

9. Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanai in view of Wilson and further in view of Wallach and further in view of U.S. Patent no. 6,085,294 ("VanDoren-94").

Regarding claim 26

Kanai, Wilson and Wallach teach a system for allocating resources but do not teach assigning at least one miss address file (MAF) value for processing I/O transactions. However, VanDoren-94 teaches at least one miss address file (MAF) (fig. 2 element 86a). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the MAF of VanDoren-94 with the system of Kanai, Wilson and Wallach because it would provide for processing I/O transactions data which has not yet completed by the CPU.

Regarding claim 27

VanDoren-94 teaches assigning a plurality of miss address file (MAF) values for processing I/O transactions (col. 7 lines 38-39, "Each CPU 12a-12d ... (MAF) 86a-86d").

Regarding claim 28

Kanai, Wilson, Wallach and VanDoren-94 teach a system for allocating resources with at least one MAF but do not teach reducing the assigned number of MAF. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to reduce or increase the number of MAF in accordance with the number of CPUs used.

10. Claims 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanai in view of Wilson and further in view of Wallach and further in view of U.S. Patent no. 6,085,276 ("VanDoren-76").

Regarding claim 29

Kanai, Wilson and Wallach teach a system for allocating resources with the I/O bridge but do not teach configuring to utilize a plurality of virtual channels to communicate with at least one processors of a multiprocessor computer system, and the resources include flow control credits associated with each of the plurality of virtual channels. However, VanDoren-76 teaches a plurality of virtual channels to communicate with the multiprocessor system, and the resources include flow control credits associated with each of the plurality of virtual channels (col. 14 line 66 to col. 15 line 5, " Virtual channels are a scheme ... among messages in the system"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the virtual channels of VanDoren-76 with the system of Kanai, Wilson and Wallach because it would provide for eliminating flow-dependence and resource dependence cycles among messages in the system in order to eliminating deadlock in the cache coherence protocol.

Regarding claim 30

VanDoren-76 teaches setting the number of flow control credits associated with each virtual channel (col. 20 lines 14-20, "flow control from the ... in the SMP system").

11. Claims 32 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallach in view of U.S. Patent No. 6,119,185 ("Westerinen").

Regarding claim 32

Wallach teaches an Input/Output (I/O) bridge for use in a computer system having a plurality of processors, the I/O bridge comprising: a plurality of I/O ports, each I/O port configured to communicate with at least one I/O device that generates or receives transactions (col. 5 lines 1-5, "a programmable mass storage adapter ... the operational computer"); resources for use in servicing the transactions of the I/O devices (col. 10 lines 57-61, "Once an adapter 310 ... configuration space registers"). Wallace does not teaches a programmable logic configured and arranged to assign the resources among the I/O ports in response to the number of I/O devices with which the I/O ports are communicating. However, Westerinen teaches a configuration logic that assign the resources among the I/O ports in response to the number of I/O devices (col. 2 lines 1-12, "processing logic that performs ... two or more devices to that resource") for the purpose of efficiently and intelligently configures to achieve enhance performance and minimize conflicts. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the logic of Westerinen with the system of Wallach because it would provide for the purpose of efficiently and intelligently configures to achieve enhance performance and minimize conflicts.

Regarding claim 41

Wallace teaches the configuration manager 500 re-assigns resources among the I/O ports dynamically while the I/O bridge continues to operate (col. 10 lines 57-61, "Once an adapter 310 ... configuration space registers").

12. Claims 33 and 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallach in view of Westerinen and further in view of Fung.

Regarding claim 33

Wallach and Westerinen teach a system for allocating resources with a configuration manager 500 but do not teach the resources comprise at least one direct memory access (DMA) engine configured to process the transactions, and the programmable logic apportions the at least one of DMA engine to process at least one transaction at a given I/O port in response to the number of I/O devices coupled to the given I/O port. However, Fung teaches at least one apportioning at least one DMA engine to process at least one transaction at a port (col. 15 lines 32-40, "The standard procedure for the ... used by their own queue") and apportioning a selected number of DMA engines to process a given transaction at a particular I/O port (col. 15 lines 37-40, "Transaction Interface 210 ... used by their own queue"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the DMA resources of Fung with the system of Wallach and Westerinen because it would provide for processing data faster in the most efficient way possible.

Regarding claim 37

Wallach teaches a system for allocating resources with a configuration manager 500 and the I/O bridge comprising at least one cache for storing information, wherein, to hot-swap an assembly

of the computer system (col. 17 lines 33-35, "the configuration manager 1100 ... that has been hotly added"), the configuration manager 500 is configured to flush the information from the at least one cache (col. 18 lines 21-27, "the FindAdapter( ) routine for an ... physical queue addresses"). Fung teaches a selected number of DMA engines to process at least one transaction at a port (col. 15 lines 32-40, "The standard procedure for the ... used by their own queue"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to disable the at least one DMA engine during the selection process of which DMA engine to be utilized.

Regarding claim 38

Fung teaches the at least one cache is one of a write cache, a read cache and a translation look-aside buffer (TLB) (col. 12 lines 27-45, "Setting the "dta" bit ... has been sent or received").

Regarding claim 39

Wallach, Westerinen and Fung do not teach the assembly is a processor. "Official Notice" is taken for both the concept and advantages of providing hot adding a processor is well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include the hot adding a processor to be part of the hot adding assembly of Wallach, Westerinen and Fung because it would provide for adding additional processing power to the existing computer system without interrupting the currently running processes.

Regarding claim 40

Wallach teaches the configuration manager 500 comprises at least one control register associated with each I/O port, and the at least one control register has a first field for apportioning (col. 10 lines 58-61, "The configuration manager 500 ... adapter's configuration space registers"). Fung

teaches at least one apportioning at least one DMA engine to process at least one transaction at a port (col. 15 lines 32-40, "The standard procedure for the ... used by their own queue").

13. Claims 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallach in view of Westerinen and further in view of U.S. Patent no. 6,085,276 ("VanDoren-76").

Regarding claim 34

Wallach and Westerinen teach a system for allocating resources but do not teach the resources include a plurality of miss address file (MAF) values for use in requesting information from the computer system, and the programmable logic sets the number of available MAF values. However, VanDoren-94 teaches assigning a plurality of miss address file (MAF) values for processing I/O transactions (col. 7 lines 38-39, "Each CPU 12a-12d ... (MAF) 86a-86d"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the MAF of VanDoren-94 with the system of Wallach and Westerinen because it would provide for processing I/O transactions data which has not yet completed by the CPU. Furthermore, it is obvious to one of ordinary skill in the art at the time the invention was made to reduce or increase the number of MAF in accordance with the number of CPUs used.

Regarding claim 35

Wallach and Westerinen teach a system for allocating resources with the I/O bridge and a configuration manager 500 but do not teach the I/O bridge communicates with the computer system through a plurality of virtual channels, the resources include a plurality of flow control credits associated with the virtual channels, and the programmable logic assigns a number of flow control credits to each virtual channel. However, VanDoren-76 teaches a plurality of virtual

channels to communicate with the multiprocessor system, and the resources include flow control credits associated with each of the plurality of virtual channels (col. 14 line 66 to col. 15 line 5, " Virtual channels are a scheme ... among messages in the system") and setting the number of flow control credits associated with each virtual channel (col. 20 lines 14-20, "flow control from the ... in the SMP system"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the virtual channels of VanDoren-76 with the system of Wallach and Westerinen because it would provide for eliminating flow-dependence and resource dependence cycles among messages in the system in order to eliminating deadlock in the cache coherence protocol.

Regarding claim 36

VanDoren-76 teaches the virtual channels comprise a Request channel, a Read I/O channel, and a Write I/O channel (col. 15 lines 16-28, "a Q0 channel for carrying ... from a processor to an IOP").

Response to Arguments

In the remarks, applicants argue that prior art fail to teach:

I. the setting of any criteria for transactions at a port, with respect to the number of devices being service via the ports as to claim 13.

II. the programmable logic configured and arranged to assign resources among I/O ports in response to the number of I/O devices with which the I/O ports are communicating as to claim 32.

In response to applicants' remarks:

I. It is noted that the examiner's position for limitations the setting of any criteria for transactions at a port is broad enough to include the system of Kanai et al. (USPN 5,864,679). Kanai et al. provides a configuration setting which enabled the ports to accept transaction packets as described below (in column 23 lines 14-28):

> A position of the type of transaction in the packet of the RPC is fixed, so that the transaction reception unit 103 which received the packet can extract the type of transaction from the received packet, and the transaction reception unit 103 supplies the extracted type of transaction to the transaction table 126. Here, it is also possible to provide a configuration in which the transaction reception unit 103 can receive the transaction packets arriving at a plurality of ports. In such a case, it is also possible to produce the transaction table for recording the information concerning the transactions arrived at that port for each port, such that when the packet is received, the transaction reception unit 103 supplies the type of transmission to the transaction table corresponding to the port from which this transaction has been received. (underlining added)

According the above cited portion, it is clear that the configuration of Kanai includes the setting of at least one criteria in order for the ports to accept transaction packets with respect to the transaction sources (devices) being service at the ports (see FIG. 4 of Kanai). It should be noted that the term "setting" is not limited to a variable setting or a fixed setting. Therefore, the limitations are meet by the reference.

II. In addition to the rejection, Prior art Westerinen et al. (USPN 6,119,185) teaches a logic that assign resources to the devices as described below (in column 1 line 66 to col. 2 line 12):

> One embodiment of the present invention includes a self-configuring computer apparatus that comprises: processing logic that performs control and data processing functions; a plurality of resources that have resource settings therefor that are coupled to said processing logic and include at least interrupts and memory; a plurality of devices which require access to one or more of said plurality of resources; and configuration logic that assigns, substantially in parallel, two or more of said plurality of devices to said resources. Another embodiment of the present invention includes similar features and configuration logic that decides the order in which two or more of said plurality of devices are assigned to one of said plurality of resources before making an assignment of those two or more devices to that resource. (underlining added)

The configuration logic of Westerinen et al. assigns resources to the devices where the devices are communicate through the I/O ports. There is nothing in the claim that limits the

assignment of resources, how to assign the resources among the I/O ports or required that the resources must directly assigned to the port . Therefore, assigning the resources to devices which connected to the ports is read on the limitations assigning the resources among the I/O ports.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner *Thomas Pham*; whose telephone number is (571) 272-3689, Monday to Thursday from 6:30 AM - 5:00 PM EST or contact Supervisor *Mr. Anthony Knight* at (571) 272-3687.

Thomas Pham
Patent Examiner

March 23, 2005

Anthony Knight
Supervisory Patent Examiner
Group 3600